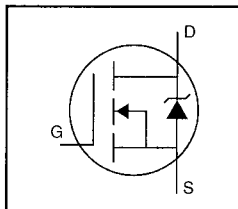


## HEXFET® Power MOSFET

- Dynamic  $dv/dt$  Rating
- Logic-Level Gate Drive
- $R_{DS(on)}$  Specified at  $V_{GS}=4V$  &  $5V$
- $175^{\circ}C$  Operating Temperature
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements



$$V_{DSS} = 60V$$

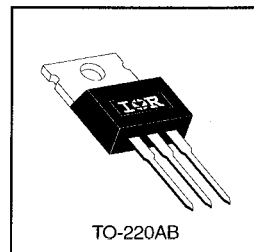
$$R_{DS(on)} = 0.028\Omega$$

$$I_D = 50^*A$$

### Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 watts. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.



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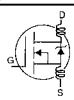
### Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D$ @ $T_C = 25^{\circ}C$	Continuous Drain Current, $V_{GS}$ @ 5.0 V	50*	A
$I_D$ @ $T_C = 100^{\circ}C$	Continuous Drain Current, $V_{GS}$ @ 5.0 V	36	
$I_{DM}$	Pulsed Drain Current ①	200	
$P_D$ @ $T_C = 25^{\circ}C$	Power Dissipation	150	W
	Linear Derating Factor	1.0	W/ $^{\circ}C$
$V_{GS}$	Gate-to-Source Voltage	$\pm 10$	V
$E_{AS}$	Single Pulse Avalanche Energy ②	400	mJ
$dv/dt$	Peak Diode Recovery $dv/dt$ ③	4.5	V/ns
$T_J$	Operating Junction and	-55 to +175	$^{\circ}C$
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds		
	Mounting Torque, 6-32 or M3 screw	10 lbf•in (1.1 N•m)	


### Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	1.0	$^{\circ}C/W$
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	—	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient	—	—	62	

## Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	60	—	—	V	$V_{GS}=0\text{V}$ , $I_D=250\mu\text{A}$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.070	—	$V/^\circ\text{C}$	Reference to $25^\circ\text{C}$ , $I_D=1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.028	$\Omega$	$V_{GS}=5.0\text{V}$ , $I_D=31\text{A}$ ④
		—	—	0.039		
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	2.0	V	$V_{DS}=V_{GS}$ , $I_D=250\mu\text{A}$
$g_{fs}$	Forward Transconductance	23	—	—	S	$V_{DS}=25\text{V}$ , $I_D=31\text{A}$ ④
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	25	$\mu\text{A}$	$V_{DS}=60\text{V}$ , $V_{GS}=0\text{V}$ $V_{DS}=48\text{V}$ , $V_{GS}=0\text{V}$ , $T_J=150^\circ\text{C}$
		—	—	250		
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS}=10\text{V}$ $V_{GS}=-10\text{V}$
	Gate-to-Source Reverse Leakage	—	—	-100		
$Q_g$	Total Gate Charge	—	—	66	nC	$I_D=51\text{A}$ $V_{DS}=48\text{V}$ $V_{GS}=5.0\text{V}$ See Fig. 6 and 13 ④
$Q_{gs}$	Gate-to-Source Charge	—	—	12		
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	—	—	43		
$t_{d(on)}$	Turn-On Delay Time	—	17	—	ns	$V_{DD}=30\text{V}$ $I_D=51\text{A}$ $R_G=4.6\Omega$ $R_D=0.56\Omega$ See Figure 10 ④
$t_r$	Rise Time	—	230	—		
$t_{d(off)}$	Turn-Off Delay Time	—	42	—		
$t_f$	Fall Time	—	110	—		
$L_D$	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact 
$L_S$	Internal Source Inductance	—	7.5	—		
$C_{iss}$	Input Capacitance	—	3300	—	pF	$V_{GS}=0\text{V}$ $V_{DS}=25\text{V}$ $f=1.0\text{MHz}$ See Figure 5
$C_{oss}$	Output Capacitance	—	1200	—		
$C_{rss}$	Reverse Transfer Capacitance	—	200	—		

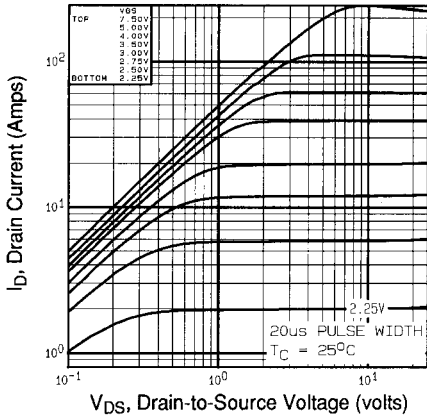
## Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	50*	A	MOSFET symbol showing the integral reverse p-n junction diode. 
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	200		
$V_{SD}$	Diode Forward Voltage	—	—	2.5	V	$T_J=25^\circ\text{C}$ , $I_S=51\text{A}$ , $V_{GS}=0\text{V}$ ④
$t_{rr}$	Reverse Recovery Time	—	130	180	ns	$T_J=25^\circ\text{C}$ , $I_F=51\text{A}$
$Q_{rr}$	Reverse Recovery Charge	—	0.84	1.3	$\mu\text{C}$	$di/dt=100\text{A}/\mu\text{s}$ ④
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S+L_D$ )				

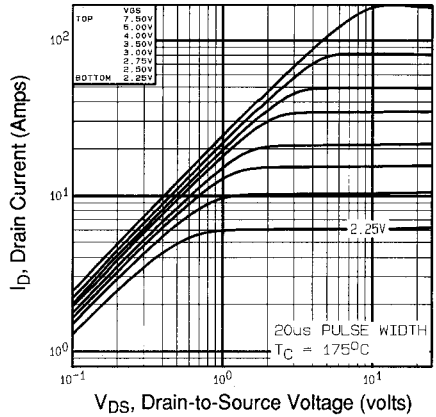
### Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)
- ②  $V_{DD}=25\text{V}$ , starting  $T_J=25^\circ\text{C}$ ,  $L=179\mu\text{H}$ ,  $R_G=25\Omega$ ,  $I_{AS}=51\text{A}$  (See Figure 12)
- ③  $I_{SD}\leq 51\text{A}$ ,  $di/dt\leq 250\text{A}/\mu\text{s}$ ,  $V_{DD}\leq V_{(BR)DSS}$ ,  $T_J\leq 175^\circ\text{C}$
- ④ Pulse width  $\leq 300\mu\text{s}$ ; duty cycle  $\leq 2\%$ .

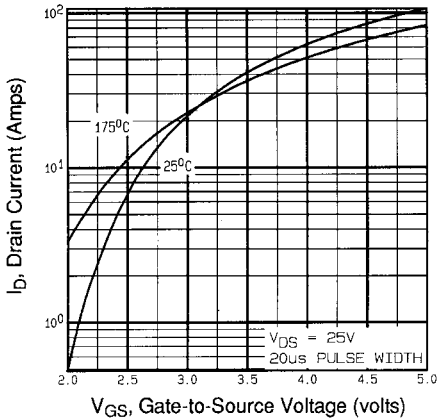
\* Current limited by the package, (Die Current =51A)



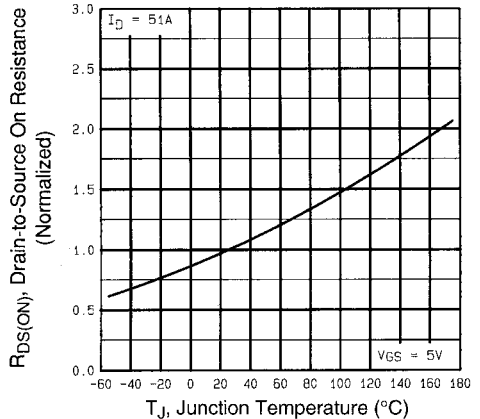
**Fig 1.** Typical Output Characteristics,  
 $T_C=25^\circ\text{C}$



**Fig 2.** Typical Output Characteristics,  
 $T_C=175^\circ\text{C}$

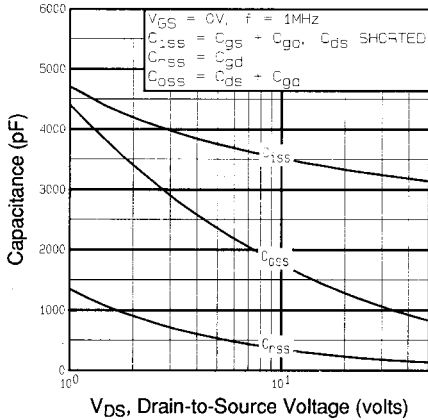


**Fig 3.** Typical Transfer Characteristics

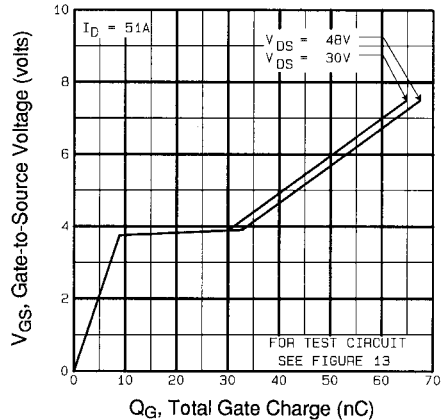


**Fig 4.** Normalized On-Resistance  
Vs. Temperature

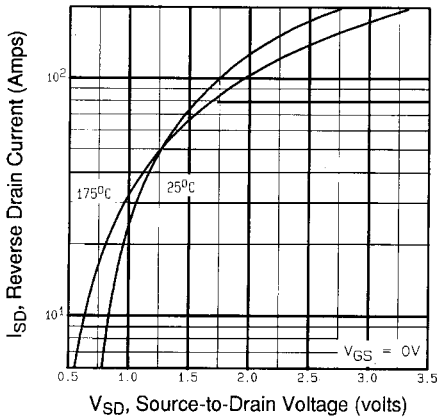
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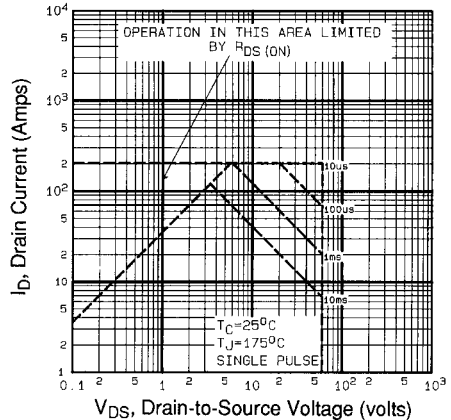
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



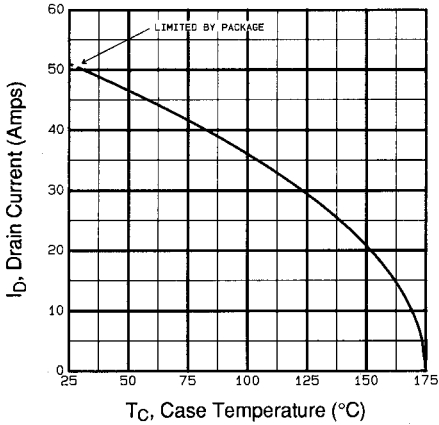
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



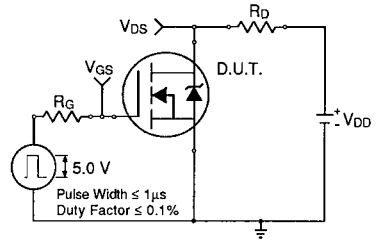
**Fig 7.** Typical Source-Drain Diode Forward Voltage



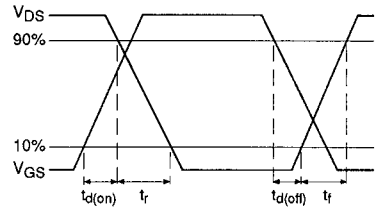
**Fig 8.** Maximum Safe Operating Area



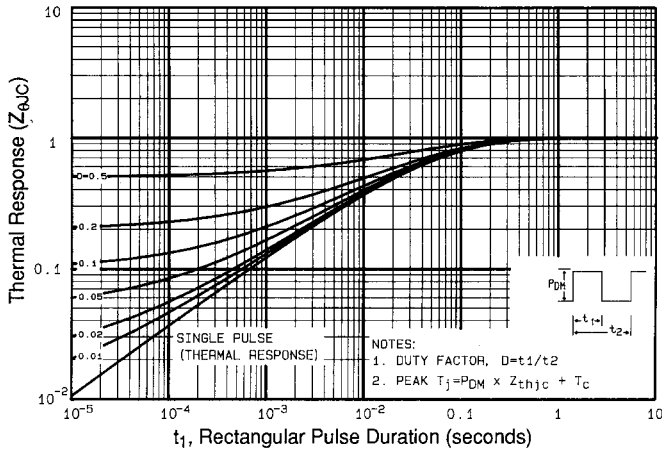
**Fig 9.** Maximum Drain Current Vs. Case Temperature



**Fig 10a.** Switching Time Test Circuit

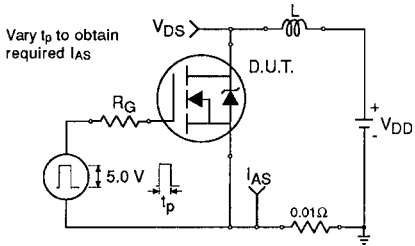


**Fig 10b.** Switching Time Waveforms

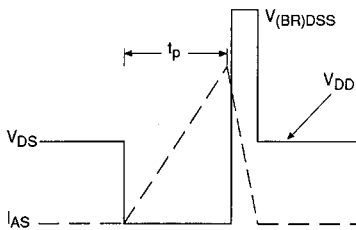


**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

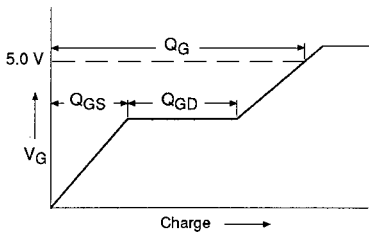
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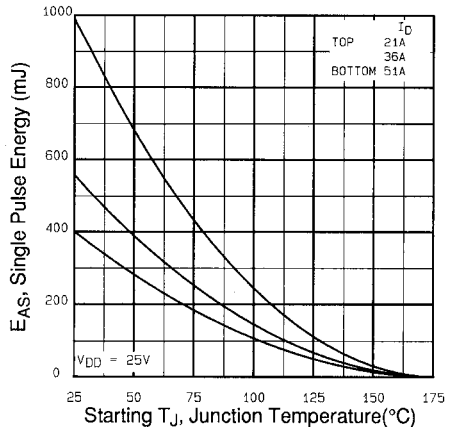
**Fig 12a.** Unclamped Inductive Test Circuit



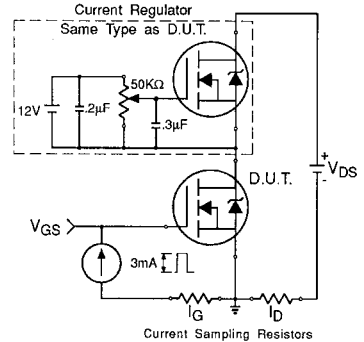
**Fig 12b.** Unclamped Inductive Waveforms



**Fig 13a.** Basic Gate Charge Waveform



**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current



**Fig 13b.** Gate Charge Test Circuit

**Appendix A:** Figure 14, Peak Diode Recovery  $dv/dt$  Test Circuit – See page 1505

**Appendix B:** Package Outline Mechanical Drawing – See page 1509

**Appendix C:** Part Marking Information – See page 1516

**Appendix E:** Optional Leadforms – See page 1525