CD4029A Types

CMOS Presettable Up/Down Counter

Binary or BCD-Decade

The RCA-CD4029A consists of a four-stage binary or BCD-decade up/down counter with provisions for look-ahead carry in both counting modes. The inputs consist of a single CLOCK, CARRY-IN (CLOCK INHIBIT), BINARY/DECADE, UP/DOWN, PRESET ENABLE, and four individual JAM signals and a CARRY OUT signal are provided as outputs.

A high PRESET ENABLE signal allows information on the JAM INPUTS to preset the counter to any state asynchronously with the clock. A low on each JAM line, when the PRESET-ENABLE signal is high, resets the counter to its zero count. The counter is advanced one count at the positive transition of the clock when the CARRY-IN and PRESET ENABLE signals are low. Advancement is inhibited when the CARRY-IN or PRESET ENABLE signals are high. The CARRY-OUT signal is normally high and goes low when the counter reaches its maximum count in the UP mode or the minimum count in the DOWN mode provided the CARRY-IN signal is low. The CARRY-IN signal in the high state can thus be considered a CLOCK INHIBIT. The CARRY-IN terminal must be connected to V_{SS} when not in use.

Binary counting is accomplished when the BINARY/DECADE input is high; the counter counts in the decade mode when the BINARY/DECADE input is low. The counter counts Up when the UP/DOWN INPUT is high, and Down when the UP/DOWN INPUT is low. Multiple packages can be connected in either a parallel-clocking or a ripple-clocking arrangement.

Parallel clocking provides synchronous control and hence faster response from all counting outputs. Ripple-clocking allows for longer clock input rise and fall times.

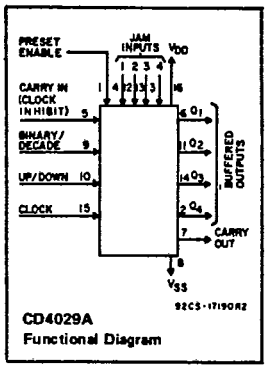
These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- Medium speed operation . . . 5 MHz (typ.) @ C_L=15 pF and $V_{DD}-V_{SS}$=10 V
- Multi-package parallel clocking for synchronous high speed output response or ripple clocking for slow clock input rise and fall times
- "Preset Enable" and individual "Jam" inputs provided
- Binary or decade up/down counting
- BCD outputs in decade mode
- Quiescent current specified to 15 V
- Maximum input leakage current of 1 μA at 15 V (full package-temperature range)
- 1-V noise margin (full package-temperature range)

Applications:

- Programmable binary and decade counting/frequency synthesizers-BCD output
- Analog to digital and digital to analog conversion
- Up/Down binary counting
- Magnitude and sign generation
- Up/Down decade counting
- Difference counting



CD4029A
Functional Diagram

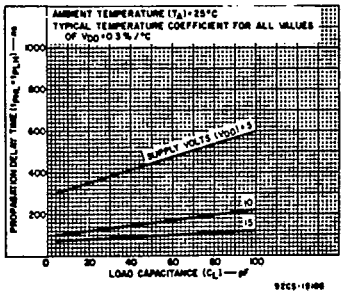


Fig. 1– Typical propagation delay time vs. C_L for Q outputs.

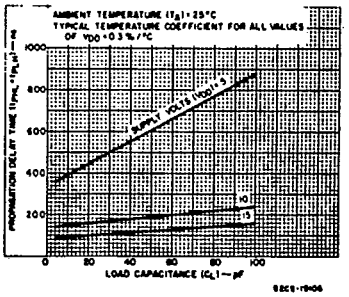


Fig. 2– Typical propagation delay time vs. C_L for carry output.

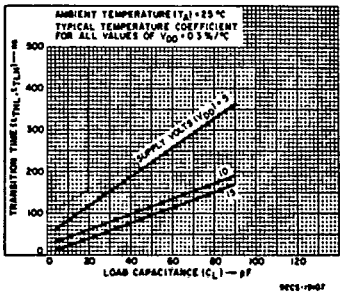


Fig. 3– Typical transition time vs. C_L for Q outputs.

RECOMMENDED OPERATING CONDITIONS at T_A=25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS D, F, K, H Packages Min.	LIMITS D, F, K, H Packages Max.	LIMITS E Package Min.	LIMITS E Package Max.	UNITS
Supply-Voltage Range (For T_A=Full Package-Temperature Range)		3	12	3	12	V
Setup Time, t_S*	5	650	–	1300	–	ns
	10	230	–	460	–	
Clock Pulse Width, t_W	5	340	–	500	–	ns
	10	170	–	250	–	
Clock Input Frequency, f_{CL}	5	dc	1.5	dc	1	MHz
	10	dc	3	dc	2	
Clock Rise or Fall Time, t_rCL,t_fCL**	5	–	15	–	15	μs
	10	–	15	–	15	
Preset Enable Pulse Width, t_W	5	330	–	660	–	ns
	10	160	–	320	–	

*From Up/Down, Binary/Decade, Carry In, or Preset Enable Control Inputs to Clock Edge.
**If more than one unit is cascaded in the parallel clocked application, t_rCL should be made less than or equal to the sum of the fixed propagation delay at 15 pF and the transition time of the carry output driving stage for the estimated capacitive load.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) ..... −65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H ..... −55 to +125°C
PACKAGE TYPE E ..... −40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) ..... −0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D):
FOR T_A=−40 to +60°C (PACKAGE TYPE E) ..... 500 mW
FOR T_A=+60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D, F, K) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) ..... Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR:
FOR T_A=FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) ..... 100 mW
INPUT VOLTAGE RANGE, ALL INPUTS ..... −0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A=25°C, Input t_r,t_f=20 ns, C_L=15 pF, R_L=200 kΩ

CHARACTERISTIC	TEST CONDITIONS V_{DD} (V)	LIMITS D, F, K, H Packages Min.	Typ.	Max.	E Package Min.	Typ.	Max.	UNITS
Clocked Operation								
Propagation Delay Time: t_{PHL}, t_{PLH} Q Outputs	5	–	325	650	–	325	1300	ns
	10	–	115	230	–	115	460	
Carry Output	5	–	425	850	–	425	1700	
	10	–	150	300	–	150	600	
Transition Time: t_{THL}, t_{TLH} Q Outputs	5	–	100	200	–	100	400	ns
	10	–	50	100	–	50	200	
Carry Output	5	–	200	400	–	200	800	
	10	–	100	200	–	100	400	
Minimum Clock Pulse Width, t_W	5	–	200	340	–	200	500	ns
	10	–	100	170	–	100	250	
Clock Rise & Fall Time, t_rCL, t_fCL**	5	–	–	15	–	–	15	μs
	10	–	–	15	–	–	15	
Minimum Setup Times, t_S*	5	–	325	650	–	325	1300	ns
	10	–	115	230	–	115	460	
Maximum Clock Input Frequency, f_{CL}	5	1.5	2.5	–	1	2.5	–	MHz
	10	3	5	–	2	5	–	
Input Capacitance, C_I	Any Input	–	5	–	–	5	–	pF
Preset Enable								
Propagation Delay Time: t_{PHL}, t_{PLH} Q Outputs	5	–	325	650	–	325	1300	ns
	10	–	115	230	–	115	460	
Carry Output	5	–	425	850	–	425	1700	
	10	–	150	300	–	150	600	
Minimum Preset Enable Pulse Width, t_W	5	–	115	330	–	115	660	ns
	10	–	80	160	–	80	320	
Minimum Preset Enable Removal Time	5	–	325	650	–	325	1300	ns
	10	–	115	230	–	115	460	
Carry Input								
Propagation Delay Time: t_{PHL}, t_{PLH} Carry Output	5	–	175	350	–	175	700	ns
	10	–	50	100	–	50	200	

For footnotes, see Recommended Operating Conditions.

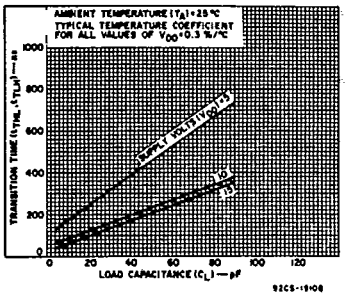


Fig. 4—Typical transition time vs. C_L for carry output.

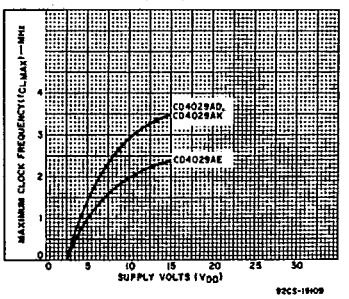


Fig. 5—Maximum clock input frequency vs. V_{DD}.

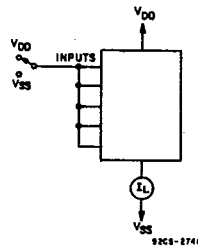


Fig. 6 — Quiescent-device-current test circuit.

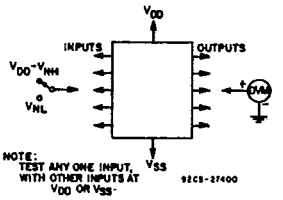


Fig. 7—Noise-immunity test circuit.

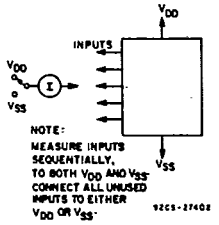


Fig. 8— Input-leakage-current test circuit.

CD4029A Types

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C)								Units
				D, F, K, H Packages				E Package				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	+25 Typ.	+25 Limit	+125	−40	+25 Typ.	+25 Limit	+85	
Quiescent Device Current, I_L Max.	–	–	5	5	0.3	5	300	50	0.5	50	700	μA
	–	–	10	10	0.5	10	600	100	1	100	1400	
	–	–	15	50	1	50	2000	500	5	500	5000	
Output Voltage: Low-Level, V_{OL}	–	5	5	0 Typ.; 0.05 Max.								V
	–	10	10	0 Typ.; 0.05 Max.								
High-Level, V_{OH}	–	0	5	4.95 Min.; 5 Typ.								
	–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	1.5 Min.; 2.25 Typ.								V
	9	–	10	3 Min.; 4.5 Typ.								
Inputs High, V_{NH}	0.8	–	5	1.5 Min.; 2.25 Typ.								
	1	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: N-Channel (Sink), I_{DN} Min.												mA
Q Outputs	0.5	–	5	0.5	0.8	0.4	0.28	0.24	0.8	0.2	0.16	
	0.5	–	10	0.74	1.2	0.6	0.42	0.36	1.2	0.3	0.24	
Carry Output	0.5	–	5	0.1	0.16	0.08	0.06	0.05	0.16	0.04	0.03	
	0.5	–	10	0.4	0.64	0.32	0.22	0.19	0.64	0.16	0.13	
P-Channel (Source), I_{DP} Min.												
Q Outputs	4.5	–	5	−0.18	−0.24	−0.12	−0.08	−0.07	−0.24	−0.06	−0.05	
	9.5	–	10	−0.3	−0.4	−0.2	−0.14	−0.14	−0.4	−0.1	−0.08	
Carry Output	4.5	–	5	−0.09	−0.12	−0.06	−0.04	−0.04	−0.12	−0.03	−0.02	
	9.5	–	10	−0.15	−0.2	−0.1	−0.07	−0.07	−0.2	−0.05	−0.04	
Input Leakage Current, I_{IL}, I_{IH}	Any Input	–	15	$\pm 10^{-5}$ Typ., ±1 Max.								μA

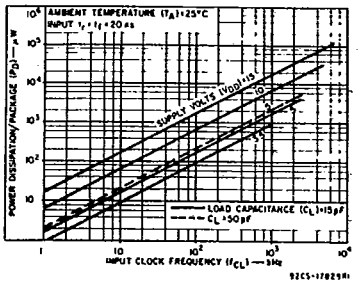


Fig. 9—Typical dissipation characteristics.

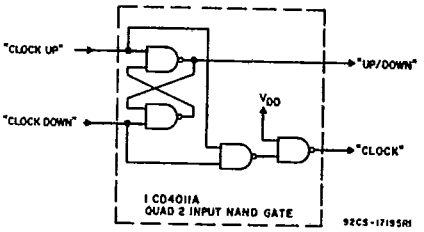
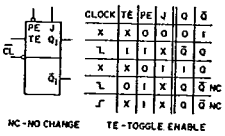
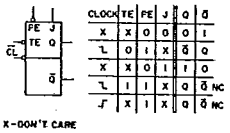


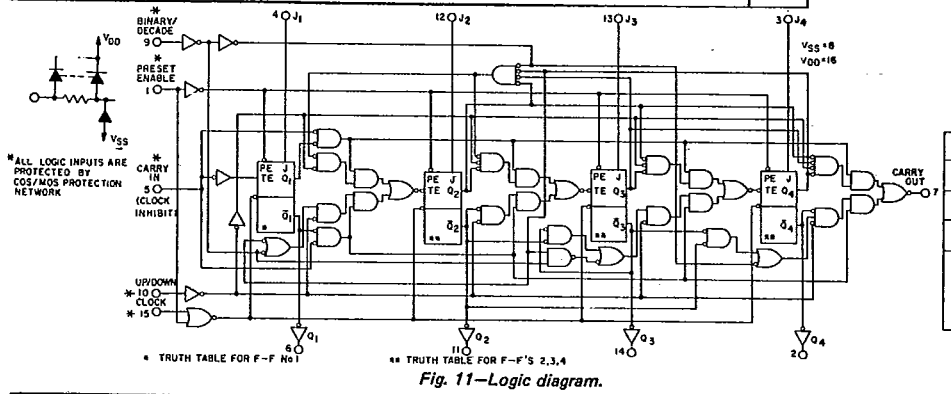
Fig. 10—Conversion of clock up, clock down input signals to clock and up/down input signals.

The CD4029A CLOCK and UP/DOWN inputs are used directly in most applications. In applications where CLOCK UP and CLOCK DOWN inputs are provided, conversion to the CD4029A CLOCK and UP/DOWN inputs can easily be realized by use of the circuit shown below.

CD4029A changes count on positive transitions of CLOCK UP or CLOCK DOWN inputs. For the gate configuration shown below, when counting up the CLOCK DOWN input must be maintained high and conversely when counting down the CLOCK UP input must be maintained high.







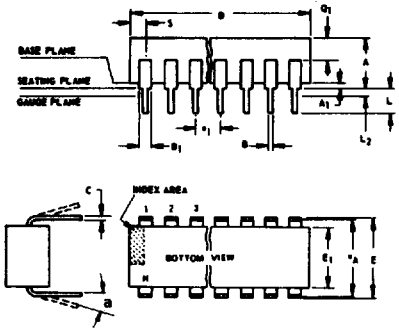
CONTROL INPUT	LOGIC LEVEL	ACTION
BIN/DEC (B/D)	1	BINARY COUNT
	0	DECADE COUNT
UP/DOWN (U/D)	1	UP COUNT
	0	DOWN COUNT
PRESET ENABLE (PE)	1	JAM IN
	0	NO JAM
CARRY IN (CI) (CLOCK INHIBIT)	1	NO COUNTER ADVANCE AT POS CLOCK TRANSITION
	0	ADVANCE COUNTER AT POS CLOCK TRANSITION

92CL-17191R3

Fig. 11—Logic diagram.

Dimensional Outlines

Dual-In-Line Welded-Seal Ceramic Packages



NOTES:
Refer to Rules for Dimensioning (JEDEC Publication No. 95) for Axial Lead Product Outlines.
1. When this device is supplied solder-dipped, the maximum lead thickness (narrow portion) will not exceed 0.013" (0.33 mm).
2. Leads within 0.005" (0.12 mm) radius of True Position (TP) at gauge plane with maximum material condition and unit installed.
3. e_A applies in zone L_2 when unit installed.
4. α applies to spread leads prior to installation.
5. N is the maximum quantity of lead positions.
6. N_1 is the quantity of allowable missing leads.

(D) SUFFIX (JEDEC MO-001-AD)
14-Lead Dual-In-Line Welded-Seal Ceramic Package

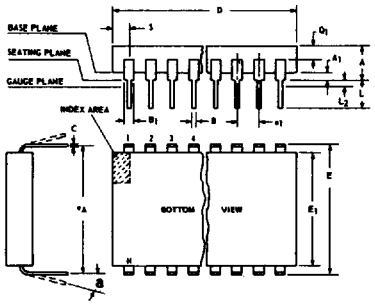
SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.120	0.160		3.05	4.06
A_1	0.020	0.065		0.51	1.65
B	0.014	0.020		0.356	0.508
B_1	0.050	0.065		1.27	1.65
C	0.008	0.012	1	0.204	0.304
D	0.745	0.770		18.93	19.55
E	0.300	0.325		7.62	8.25
E_1	0.240	0.260		6.10	6.60
e_1	0.100 TP		2	2.54 TP	
e_A	0.300 TP		2, 3	7.62 TP	
L	0.125	0.150		3.18	3.81
L_2	0.000	0.030		0.000	0.76
α	0°	15°	4	0°	15°
N	14		5	14	
N_1	0		6	0	
Q_1	0.050	0.085		1.27	2.15
S	0.065	0.090		1.66	2.28

92SS-4411R2

(D) SUFFIX (JEDEC MO-001-AE)
16-Lead Dual-In-Line Welded-Seal Ceramic Package

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.120	0.160		3.05	4.06
A_1	0.020	0.065		0.51	1.65
B	0.014	0.020		0.356	0.508
B_1	0.035	0.065		0.89	1.65
C	0.008	0.012	1	0.204	0.304
D	0.745	0.785		18.93	19.93
E	0.300	0.325		7.62	8.25
E_1	0.240	0.260		6.10	6.60
e_1	0.100 TP		2	2.54 TP	
e_A	0.300 TP		2, 3	7.62 TP	
L	0.125	0.150		3.18	3.81
L_2	0.000	0.030		0.000	0.76
α	0°	15°	4	0°	15°
N	16		5	16	
N_1	0		6	0	
Q_1	0.050	0.085		1.27	2.15
S	0.015	0.060		0.39	1.52

92SS-4286R5



NOTES:
Refer to Rules for Dimensioning (JEDEC Publication No. 95) for Axial Lead Product Outlines.
1. When this device is supplied solder-dipped, the maximum lead thickness (narrow portion) will not exceed 0.013" (0.33 mm).
2. Leads within 0.005" (0.12 mm) radius of True Position (TP) at gauge plane with maximum material condition and unit installed.
3. e_A applies in zone L_2 when unit installed.
4. α applies to spread leads prior to installation.
5. N is the maximum quantity of lead positions.
6. N_1 is the quantity of allowable missing leads.

(D) SUFFIX (JEDEC MO-015-AG)
24-Lead Dual-In-Line Welded-Seal Ceramic Package

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.090	0.200		2.29	5.08
A_1	0.020	0.070		0.51	1.78
B	0.015	0.020		0.381	0.508
B_1	0.045	0.055		1.143	1.397
C	0.008	0.012	1	0.204	0.304
D	1.15	1.22		29.21	30.98
E	0.600	0.625		15.24	15.87
E_1	0.480	0.520		12.20	13.20
e_1	0.100 TP		2	2.54 TP	
e_A	0.600 TP		2,3	15.24 TP	
L	0.100	0.180		2.54	4.57
L_2	0.000	0.030		0.00	0.76
α	0°	15°	4	0°	15°
N	24		5	24	
N_1	0		6	0	
Q_1	0.020	0.080		0.51	2.03
S	0.020	0.060		0.51	1.52

92CS-19948R4

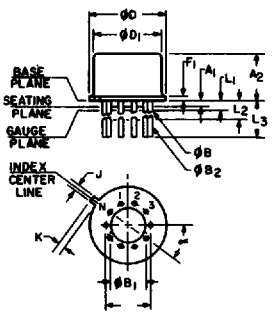
(D) SUFFIX (JEDEC MO-015-AH)
28-Lead Dual-In-Line Welded-Seal Ceramic Package

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.090	0.200		2.29	5
A_1	0	0.070	2	0	1.77
B	0.015	0.020		0.381	0.508
B_1	0.015	0.055		0.39	1.39
C	0.008	0.012	1	0.204	0.304
D	1.380	1.420		35.06	36.06
E	0.600	0.625		15.24	15.87
E_1	0.485	0.515		12.32	13.08
e_1	0.100 TP		2	2.54 TP	
e_A	0.600 TP		2,3	15.24 TP	
L	0.100	0.200		2.8	5
L_2	0	0.030		0	0.76
α	0°	15°	4	0°	15°
N	28		5	28	
N_1	0		6	0	
Q_1	0.020	0.070		0.51	1.77
S	0.040	0.070		1.02	1.77

92CM-20250R2

TO-5 Style Package

(T) SUFFIX (JEDEC MO-006-AG)
12-Lead Metal Package



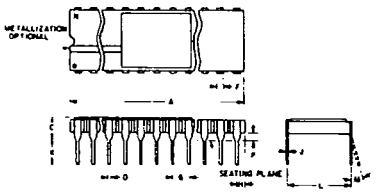
92CS-19774

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
a	0.230		2	5.84 TP	
A_1	0	0		0	0
A_2	0.165	0.185		4.19	4.70
ϕB	0.016	0.019	3	0.407	0.482
ϕB_1	0	0		0	0
ϕB_2	0.016	0.021	3	0.407	0.533
ϕD	0.335	0.370		8.51	9.39
ϕD_1	0.305	0.335		7.75	8.50
F_1	0.020	0.040		0.51	1.01
j	0.028	0.034		0.712	0.863
k	0.029	0.045	4	0.74	1.14
L_1	0.000	0.050	3	0.00	1.27
L_2	0.250	0.500	3	6.4	12.7
L_3	0.500	0.562	3	12.7	14.27
α	30° TP			30° TP	
N	12		6	12	
N_1	1		5	1	

NOTES:
1. Refer to Rules for Dimensioning Axial Lead Product Outlines.
2. Leads at gauge plane within 0.007" (0.178 mm) radius of True Position (TP) at maximum material condition.
3. ϕB applies between L_1 and L_2. ϕB_2 applies between L_2 and 0.500" (12.70 mm) from seating plane. Diameter is uncontrolled in L_1 and beyond 0.500" (12.70 mm).
4. Measure from Max. ϕD.
5. N_1 is the quantity of allowable missing leads.
6. N is the maximum quantity of lead positions.

Dimensional Outlines (Cont'd)

DUAL-IN-LINE SIDE-BRAZED CERAMIC PACKAGES



NOTES:
1. Leads within 0.005" (0.13 mm)-radius of True Position at maximum material condition.
2. Dimension "L" to center of leads when formed parallel.
3. When this device is supplied solder-dipped, the maximum lead thickness (narrow portion) will not exceed 0.013" (0.33 mm).

(D) SUFFIX
18-Lead Dual-In-Line
Side-Brazed Ceramic Package

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.890	0.915		22.606	23.241
C	–	0.200		–	5.080
D	0.015	0.021		0.381	0.533
F	0.054 REF.		1	1.371 REF.	
G	0.100 BSC		1	2.54 BSC	
H	0.035	0.065		0.889	1.651
J	0.008	0.012	3	0.203	0.304
K	0.125	0.150		3.175	3.810
L	0.290	0.310	2	7.366	7.874
M	0°	15°		0°	15°
P	0.025	0.045		0.635	1.143
N	18			18	

92CS-27231R1

(D) SUFFIX
22-Lead Dual-In-Line
Side-Brazed Ceramic Package

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	1.065	1.100		27.05	27.94
C	0.085	0.145		2.16	3.68
D	0.017	0.023		0.43	0.58
F	0.040 REF.		1	1.02 REF.	
G	0.100 BSC		1	2.54 BSC	
H	0.030	0.070		0.76	1.78
J	0.008	0.012	3	0.20	0.30
K	0.125	0.175		3.18	4.45
L	0.380	0.420	2	9.65	10.67
M	–	7°		–	7°
P	0.025	0.050		0.64	1.27
N	22			22	

92CS-25186R2

(D) SUFFIX
24-Lead Dual-In-Line
Side-Brazed Ceramic Package

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	1.180	1.220		29.98	30.98
C	0.085	0.145		2.16	3.68
D	0.015	0.023		0.39	0.58
F	0.040 REF.			1.02 REF.	
G	0.100 BSC		1	2.54 BSC	
H	0.030	0.070		0.77	1.77
J	0.008	0.012	3	0.21	0.30
K	0.125	0.175		3.18	4.44
L	0.580	0.620	2	14.74	15.74
M	–	7°		–	7°
P	0.025	0.050		0.64	1.27
N	24			24	

92CS-30986R1

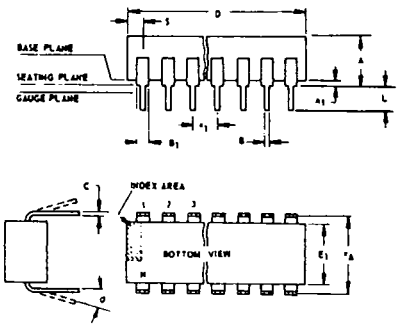
(D) SUFFIX
40-Lead Dual-In-Line
Side-Brazed Ceramic Package

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	1.980	2.020		50.30	51.30
C	0.095	0.155		2.43	3.93
D	0.017	0.023		0.43	0.56
F	0.050 REF.			1.27 REF.	
G	0.100 BSC		1	2.54 BSC	
H	0.030	0.070		0.76	1.78
J	0.008	0.012	3	0.20	0.30
K	0.125	0.175		3.18	4.45
L	0.580	0.620	2	14.74	15.74
M	–	7°		–	7°
P	0.025	0.050		0.64	1.27
N	40			40	

92CM-27029R2

Dual-In-Line Plastic and Frit-Seal Ceramic Packages

(E) SUFFIX (JEDEC MO-001-AN)
8-Lead Dual-In-Line Plastic
(Mini-DIP) Package



SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.155	0.200		3.94	5.08
A_1	0.020	0.050		0.508	1.27
B	0.014	0.020		0.356	0.508
B_1	0.035	0.065		0.889	1.65
C	0.008	0.012	1	0.203	0.304
D	0.370	0.400		9.40	10.16
E	0.300	0.325		7.62	8.25
E_1	0.240	0.260		6.10	6.60
e_1	0.100 TP		2	2.54 TP	
e_A	0.300 TP		2, 3	7.62 TP	
L	0.125	0.150		3.18	3.81
L_2	0.000	0.030		0.000	0.762
α	0	15	4	0	15
N	8		5	8	
N_1	0		6	0	
Q_1	0.040	0.075		1.02	1.90
S	0.015	0.060		0.381	1.52

92CS-24026R1

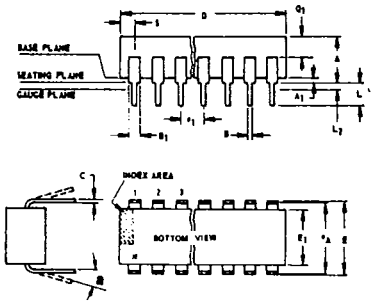
NOTES:

Refer to Rules for Dimensioning (JEDEC Publication No. 95) for Axial Lead Product Outlines.

1. When this device is supplied solder-dipped, the maximum lead thickness (narrow portion) will not exceed 0.013".
2. Leads within 0.005" (0.12 mm) radius of True Position (TP) at guage plane with maximum material condition and unit installed.
3. e_A applies in zone L_2 when unit installed.
4. α applies to spread leads prior to installation.
5. N is the maximum quantity of lead positions.
6. N_1 is the quantity of allowable missing leads.

Dimensional Outlines (Cont'd)

Dual-In-Line Plastic and Frit-Seal Ceramic Packages (Cont'd)



NOTES:
Refer to Rules for Dimensioning (JEDEC Publication No. 95) for Axial Lead Product Outlines.
1. When this device is supplied solder dipped, the maximum lead thickness (narrow portion) will not exceed 0.013" (0.33 mm).
2. Leads within 0.005" (0.12 mm) radius of True Position (TP) at gauge plane with maximum material condition and unit installed.
3. e_A applies in zone L_2 when unit installed.
4. α applies to spread leads prior to installation.
5. N is the maximum quantity of lead positions.
6. N_1 is the quantity of allowable missing leads.

(E) and (F) SUFFIXES (JEDEC MO-001-AB)
14-Lead Dual-In-Line Plastic or Frit-Seal Ceramic Package

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.155	0.200		3.94	5.08
A_1	0.020	0.060		0.51	1.27
B	0.014	0.020		0.356	0.508
B_1	0.050	0.065		1.27	1.65
C	0.008	0.012	1	0.204	0.304
D	0.745	0.770		18.93	19.55
E	0.300	0.325		7.62	8.25
E_1	0.240	0.260		6.10	6.60
e_1	0.100 TP		2	2.54 TP	
e_A	0.300 TP		2, 3	7.62 TP	
L	0.125	0.150		3.18	3.81
L_2	0.000	0.030		0.000	0.76
a	0°	15°	4	0°	15°
N	14		5	14	
N_1	0		6	0	
Q_1	0.040	0.075		1.02	1.90
S	0.065	0.090		1.66	2.28

92SS-4296R3

(E) and (F) SUFFIXES (JEDEC MO-001-AC)
16-Lead Dual-In-Line Plastic or Frit-Seal Ceramic Package

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.155	0.200		3.94	5.08
A_1	0.020	0.050		0.51	1.27
B	0.014	0.020		0.356	0.508
B_1	0.035	0.065		0.89	1.65
C	0.008	0.012	1	0.204	0.304
D	0.745	0.785		18.93	19.93
E	0.300	0.325		7.62	8.25
E_1	0.240	0.260		6.10	6.60
e_1	0.100 TP		2	2.54 TP	
e_A	0.300 TP		2, 3	7.62 TP	
L	0.125	0.150		3.18	3.81
L_2	0.000	0.030		0.000	0.76
a	0°	15°	4	0°	15°
N	16		5	16	
N_1	0		6	0	
Q_1	0.040	0.075		1.02	1.90
S	0.015	0.060		0.39	1.52

92CM-15967R4

(E) SUFFIX
18-Lead Dual-In-Line Plastic Package

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.155	0.200		3.94	5.08
A_1	0.020	0.050		0.508	1.27
B	0.014	0.020		0.356	0.508
B_1	0.035	0.065		0.89	1.65
C	0.008	0.012	1	0.204	0.304
D	0.845	0.885		21.47	22.47
E_1	0.240	0.260		6.10	6.60
e_1	0.100 TP		2	2.54 TP	
e_A	0.300 TP		2,3	7.62 TP	
L	0.125	0.150		3.18	3.81
a	0°	15°	4	0°	15°
N	18		5	18	
N_1	0		6	0	
S	0.015	0.060		0.39	1.52

92CS-30630

(E) SUFFIX
22-Lead Dual-In-Line Plastic Package

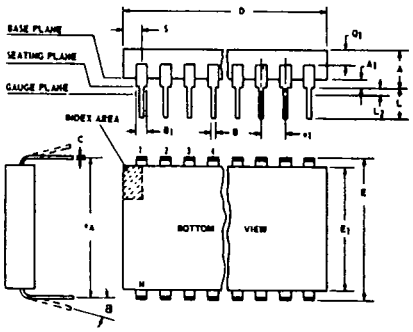
SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.155	0.200		3.94	5.08
A_1	0.020	0.050		0.508	1.27
B	0.015	0.020		0.381	0.508
B_1	0.035	0.065		0.89	1.65
C	0.008	0.012	1	0.204	0.304
D		1.120			28.44
E	0.390	0.420		9.91	10.66
E_1	0.345	0.355		8.77	9.01
e_1	0.100 TP		2	2.54 TP	
e_A	0.400 TP		2, 3	10.16 TP	
L	0.125	0.150		3.18	3.81
L_2	0	0.030		0	0.762
a	2°	15°	4	2°	15°
N	22		5	22	
N_1	0		6	0	
Q_1	0.055	0.085		1.40	2.15
S	0.015	0.060		0.381	1.27

92CS-30830

(F) SUFFIX (JEDEC MO-001-AG)
16-Lead Dual-In-Line Frit-Seal Ceramic Package

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.165	0.210		4.20	5.33
A_1	0.015	0.045		0.381	1.14
B	0.015	0.020		0.381	0.508
B_1	0.045	0.070		1.15	1.77
C	0.009	0.011	1	0.229	0.279
D	0.750	0.795		19.05	20.19
E	0.295	0.325		7.50	8.25
E_1	0.245	0.300		6.23	7.62
e_1	0.100 TP		2	2.54 TP	
e_A	0.300 TP		2, 3	7.62 TP	
L	0.120	0.160		3.05	4.06
L_2	0.000	0.030		0.000	0.76
a	2°	15°	4	2°	15°
N	16		5	16	
N_1	0		6	0	
Q_1	0.050	0.080		1.27	2.03
S	0.010	0.060		0.254	1.52

92CM-22284R1



NOTES:
Refer to Rules for Dimensioning (JEDEC Publication No. 95) for Axial Lead Product Outlines.
1. When this device is supplied solder dipped, the maximum lead thickness (narrow portion) will not exceed 0.013".
2. Leads within 0.005" (0.12 mm) radius of True Position (TP) at guage plane with maximum material condition and unit installed
3. e_A applies in zone L_2 when unit installed.
4. α applies to spread leads prior to installation.
5. N is the maximum quantity of lead positions.
6. N_1 is the quantity of allowable missing leads.

(E) and (F) SUFFIXES (JEDEC MO-015-AA)
24-Lead Dual-In-Line Plastic or Frit-Seal Ceramic Package

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.120	0.250		3.10	6.30
A_1	0.020	0.070		0.51	1.77
B	0.016	0.020		0.407	0.508
B_1	0.028	0.070		0.72	1.77
C	0.008	0.012	1	0.204	0.304
D	1.20	1.29		30.48	32.76
E	0.600	0.625		15.24	15.87
E_1	0.515	0.580		13.09	14.73
e_1	0.100 TP		2	2.54 TP	
e_A	0.600 TP		2,3	15.24 TP	
L	0.100	0.200		2.54	5.00
L_2	0.000	0.030		0.00	0.76
a	0°	15°	4	0°	15°
N	24		5	24	
N_1	0		6	0	
Q_1	0.040	0.075		1.02	1.90
S	0.040	0.100		1.02	2.54

92CS26938R2

(E) SUFFIX
40-Lead Dual-In-Line Plastic Package

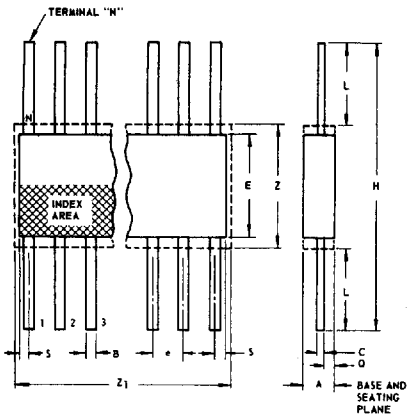
SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.120	0.250		3.10	6.30
A_1	0.020	0.070		0.51	1.77
B	0.016	0.020		0.407	0.508
B_1	0.028	0.070		0.72	1.77
C	0.008	0.012	1	0.204	0.304
D	2.000	2.090		50.80	53.09
E_1	0.515	0.580		13.09	14.73
e_1	0.100 TP		2	2.54 TP	
e_A	0.600 TP		2,3	15.24 TP	
L	0.100	0.200		2.54	5.00
L_2	0.000	0.030		0.00	0.76
a	0°	15°	4	0°	15°
N	40		5	40	
N_1	0		6	0	
Q_1	0.065	0.095		1.66	2.41
S	0.040	0.100		1.02	2.54

92CS-30959

Dimensional Outlines (Cont'd)

Ceramic Flat Packs

(K) SUFFIX (JEDEC MO-004-AF)
14-Lead



SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.008	0.100		0.21	2.54
B	0.015	0.019	1	0.381	0.482
C	0.003	0.006	1	0.077	0.152
e	0.050 TP		2	1.27 TP	
E	0.200	0.300		5.1	7.6
H	0.600	1.000		15.3	25.4
L	0.150	0.350		3.9	8.8
N	14		3	14	
Q	0.005	0.050		0.13	1.27
S	0.000	0.050		0.00	1.27
Z	0.300		4	7.62	
Z_1	0.400		4	10.16	

92SS-4300R3

NOTES:
1. Refer to JEDEC Publication No. 95 for Rules for Dimensioning Peripheral Lead Outlines.
2. Leads within 0.005" (0.12 mm) radius of True Position (TP) at maximum material condition.
3. N is the maximum quantity of lead positions.
4. Z and Z_1 determine a zone within which all body and lead irregularities lie.

(K) SUFFIX (JEDEC MO-004-AG)
16-Lead

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.008	0.100		0.21	2.54
B	0.015	0.019	1	0.381	0.482
C	0.003	0.006	1	0.077	0.152
e	0.050 TP		2	1.27 TP	
E	0.200	0.300		5.1	7.6
H	0.600	1.000		15.3	25.4
L	0.150	0.350		3.9	8.8
N	16		3	16	
Q	0.005	0.050		0.13	1.27
S	0.000	0.025		0.00	0.63
Z	0.300		4	7.62	
Z_1	0.400		4	10.16	

92CS-17271R3

(K) SUFFIX
24-Lead

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.075	0.120		1.91	3.04
B	0.018	0.022	1	0.458	0.558
C	0.004	0.007	1	0.102	0.177
e	0.050 TP		2	1.27 TP	
E	0.600	0.700		15.24	17.78
H	1.150	1.350		29.21	34.29
L	0.225	0.325		5.72	8.25
N	24		3	24	
Q	0.035	0.070		0.89	1.77
S	0.060	0.110	1	1.53	2.79
Z	0.700		4	17.78	
Z_1	0.750		4	19.05	

92CS-19949R2

(K) SUFFIX
28-Lead

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.075	0.120		1.91	3.04
B	0.018	0.022	1	0.458	0.558
C	0.004	0.007	1	0.102	0.177
e	0.050 TP		2	1.27 TP	
E	0.600	0.700		15.24	17.78
H	1.150	1.350		29.21	34.29
L	0.225	0.325		5.72	8.25
N	28		3	28	
Q	0.035	0.070		0.89	1.77
S	0	0.060	1	0	1.53
Z	0.700		4	17.78	
Z_1	0.750		4	19.05	

92CS-20972