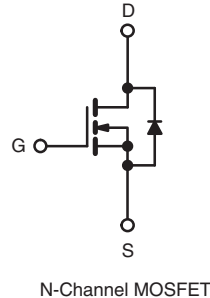
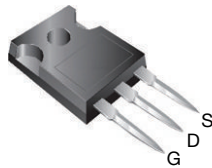


E Series Power MOSFET

PRODUCT SUMMARY	
V_{DS} (V) at T_J max.	650
$R_{DS(on)}$ max. at 25 °C (Ω)	$V_{GS} = 10$ V 0.125
Q_g max. (nC)	130
Q_{gs} (nC)	15
Q_{gd} (nC)	39
Configuration	Single

TO-247AC


FEATURES

- Low figure-of-merit (FOM) $R_{on} \times Q_g$
- Low input capacitance (C_{iss})
- Reduced switching and conduction losses
- Ultra low gate charge (Q_g)
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE
Available

APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
 - High-intensity discharge (HID)
 - Fluorescent ballast lighting
 - LED lighting
- Industrial
 - Welding
 - Induction heating
 - Motor drives
- Battery chargers
- Renewable energy
 - Solar (PV inverters)


ORDERING INFORMATION	
Package	TO-247AC
Lead (Pb)-free	SiHG30N60E-E3
Lead (Pb)-free and Halogen-free	SiHG30N60E-GE3

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	600	V
Gate-Source Voltage	V_{GS}	± 30	
Continuous Drain Current ($T_J = 150$ °C)	V_{GS} at 10 V	$T_C = 25$ °C	A
		$T_C = 100$ °C	
Pulsed Drain Current ^a	I_{DM}	65	
Linear Derating Factor		2	W/°C
Single Pulse Avalanche Energy ^b	E_{AS}	690	mJ
Maximum Power Dissipation	P_D	250	W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +150	°C
Drain-Source Voltage Slope	dV/dt	$V_{DS} = 0$ V to 80 % V_{DS}	V/ns
Reverse Diode dV/dt ^d		18	
Soldering Recommendations (Peak Temperature) ^c	for 10 s	300	°C

Notes

- Repetitive rating; pulse width limited by maximum junction temperature.
- $V_{DD} = 50$ V, starting $T_J = 25$ °C, $L = 28.2$ mH, $R_g = 25$ Ω , $I_{AS} = 7$ A.
- 1.6 mm from case.
- $I_{SD} \leq I_D$, $dI/dt = 100$ A/ μ s, starting $T_J = 25$ °C.

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	62	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	0.5	

SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	600	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}, I_D = 250\text{ }\mu\text{A}$	-	0.64	-	V/°C
Gate-Source Threshold Voltage (N)	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.0	2.8	4.0	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20\text{ V}$	-	-	± 100	nA
		$V_{GS} = \pm 30\text{ V}$	-	-	± 1	μA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$	-	-	1	μA
		$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}, T_J = 150\text{ }^\circ\text{C}$	-	-	100	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 15\text{ A}$	-	0.104	0.125	Ω
Forward Transconductance ^a	g_{fs}	$V_{DS} = 8\text{ V}, I_D = 3\text{ A}$	-	5.4	-	S
Dynamic						
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, V_{DS} = 100\text{ V}, f = 1.0\text{ MHz}$	-	2600	-	pF
Output Capacitance	C_{oss}		-	138	-	
Reverse Transfer Capacitance	C_{rss}		-	3	-	
Effective Output Capacitance, Energy Related ^a	$C_{o(er)}$		$V_{DS} = 0\text{ V to } 480\text{ V}, V_{GS} = 0\text{ V}$	-	98	
Effective Output Capacitance, Time Related ^b	$C_{o(tr)}$		-	346	-	
Total Gate Charge	Q_g	$V_{GS} = 10\text{ V}, I_D = 15\text{ A}, V_{DS} = 480\text{ V}$	-	85	130	nC
Gate-Source Charge	Q_{gs}		-	15	-	
Gate-Drain Charge	Q_{gd}		-	39	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 380\text{ V}, I_D = 15\text{ A}, V_{GS} = 10\text{ V}, R_g = 4.7\text{ }\Omega$	-	19	40	ns
Rise Time	t_r		-	32	65	
Turn-Off Delay Time	$t_{d(off)}$		-	63	95	
Fall Time	t_f		-	36	75	
Gate Input Resistance	R_g	$f = 1\text{ MHz}, \text{open drain}$	-	0.63	-	Ω
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	29	A
Pulsed Diode Forward Current	I_{SM}		-	-	65	
Diode Forward Voltage	V_{SD}	$T_J = 25\text{ }^\circ\text{C}, I_S = 15\text{ A}, V_{GS} = 0\text{ V}$	-	-	1.3	V
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}, I_F = I_S = 15\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, V_R = 20\text{ V}$	-	402	605	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	7	15	μC
Reverse Recovery Current	I_{RRM}		-	32	65	A

Notes

- a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} .
 b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} .

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

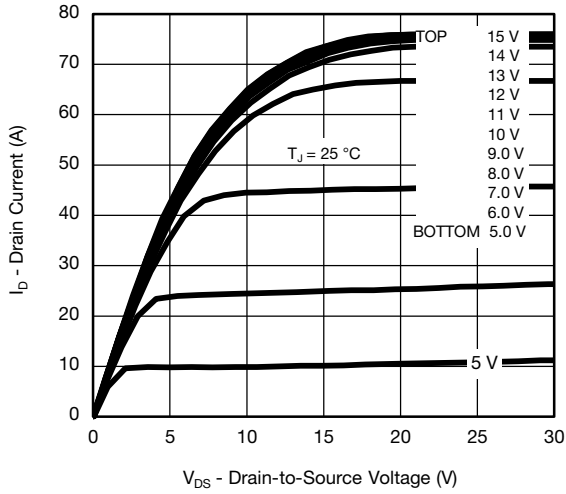


Fig. 1 - Typical Output Characteristics, $T_C = 25\text{ }^\circ\text{C}$

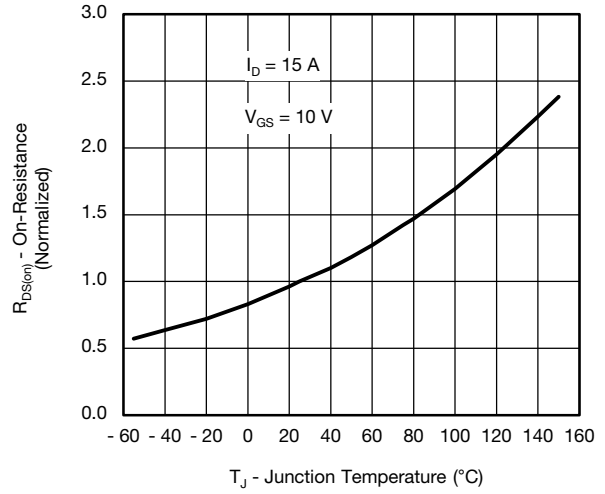


Fig. 4 - Normalized On-Resistance vs. Temperature

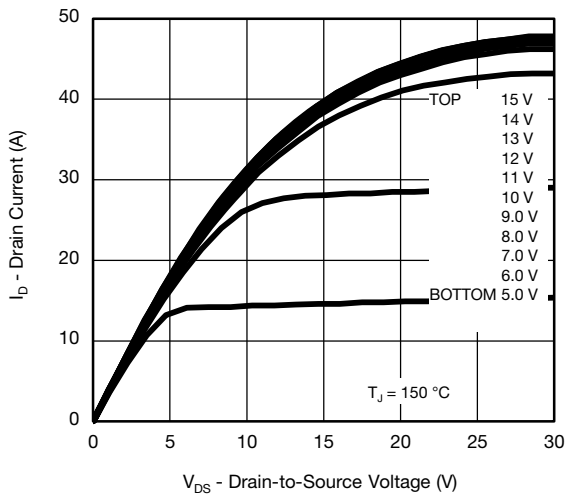


Fig. 2 - Typical Output Characteristics, $T_C = 150\text{ }^\circ\text{C}$

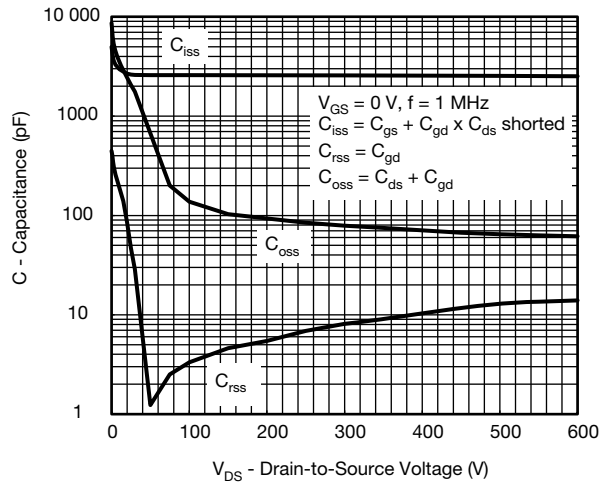


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

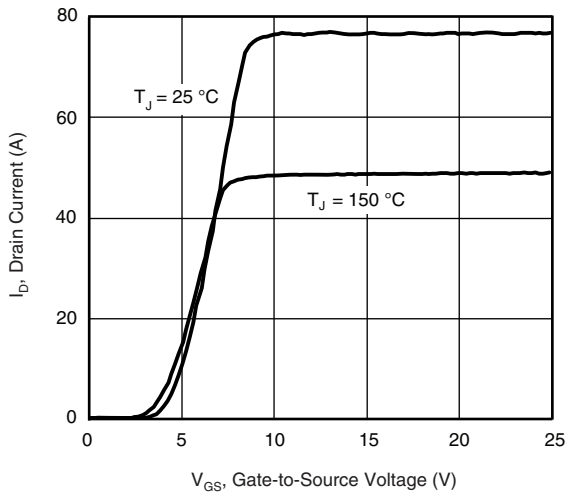


Fig. 3 - Typical Transfer Characteristics

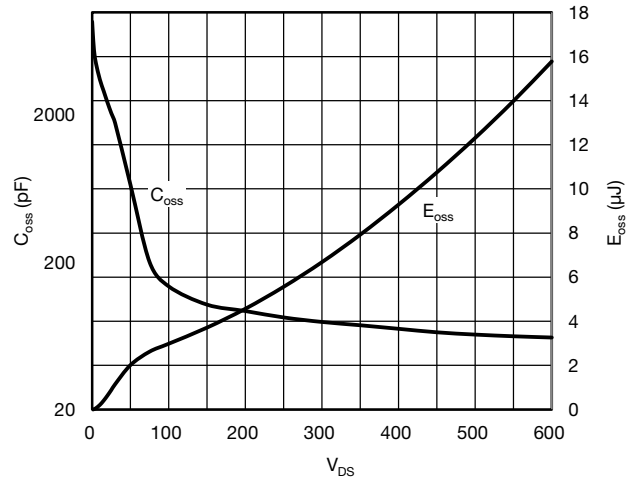


Fig. 6 - C_{oss} and E_{oss} vs. V_{DS}

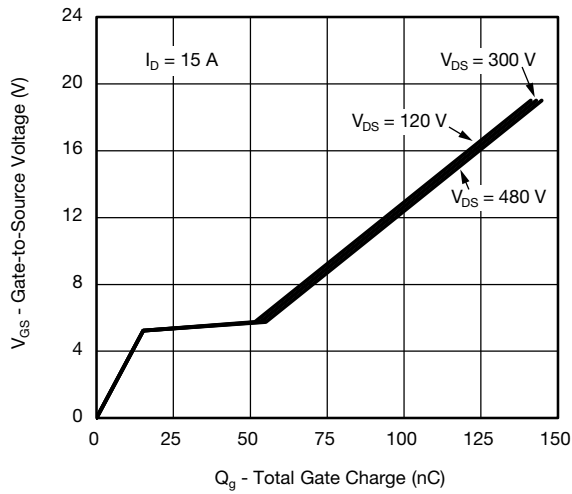


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

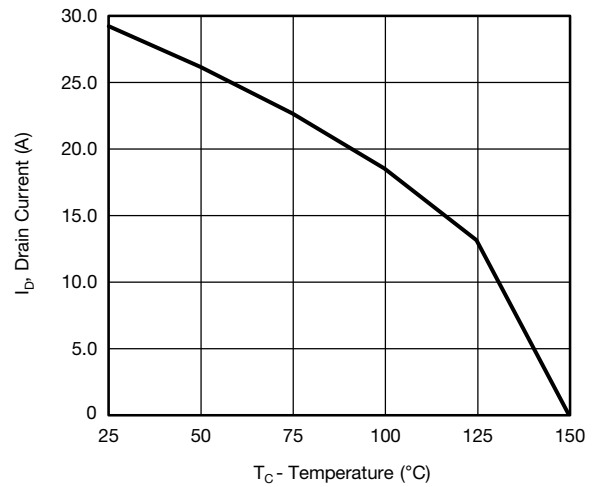


Fig. 10 - Maximum Drain Current vs. Case Temperature

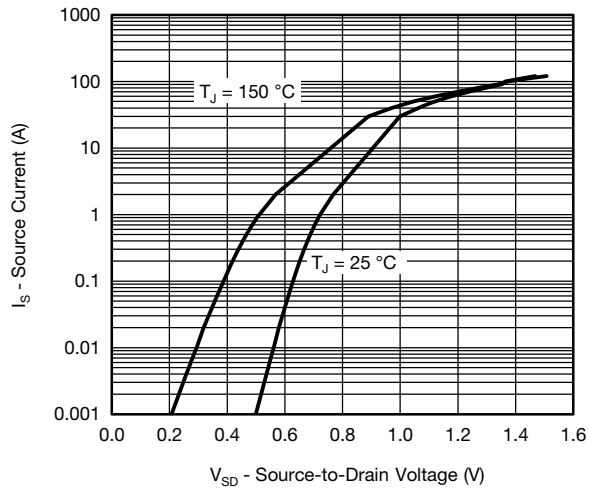


Fig. 8 - Typical Source-Drain Diode Forward Voltage

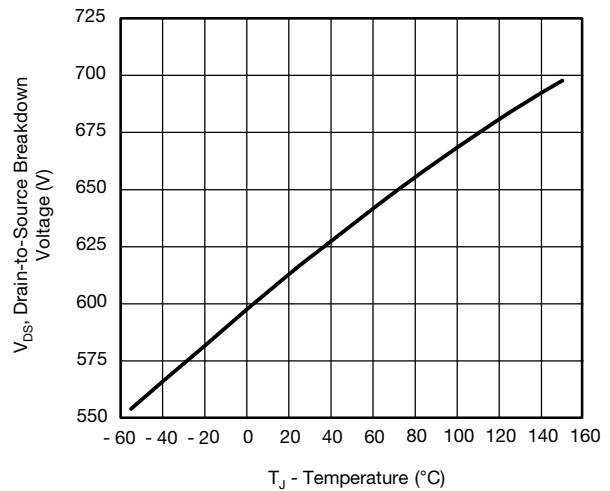


Fig. 11 - Temperature vs. Drain-to-Source Voltage

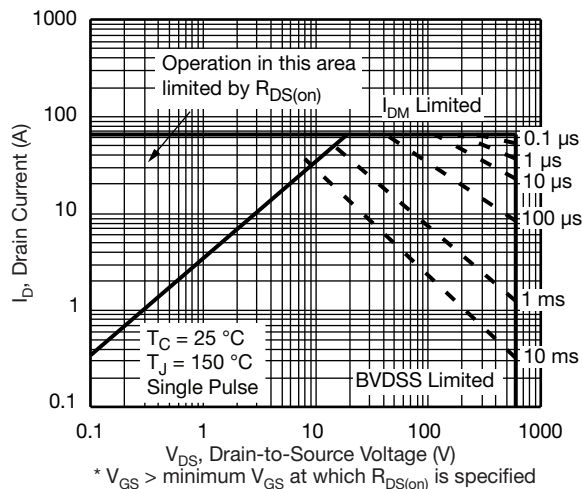


Fig. 9 - Maximum Safe Operating Area

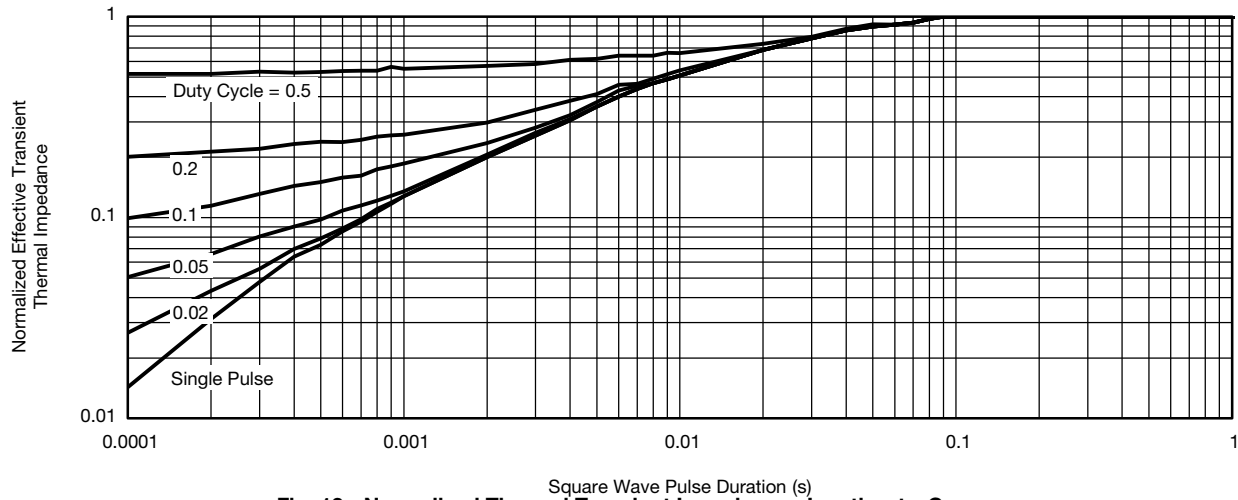


Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case

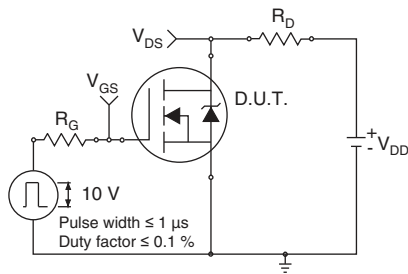


Fig. 13 - Switching Time Test Circuit

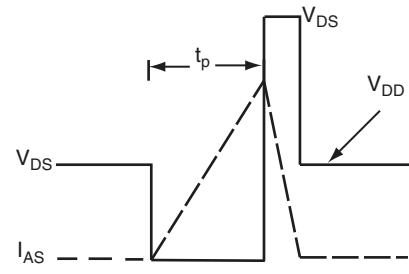


Fig. 16 - Unclamped Inductive Waveforms

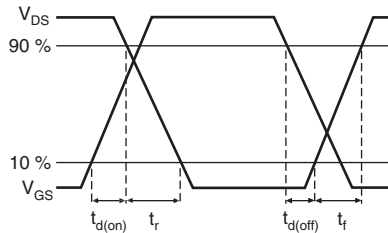


Fig. 14 - Switching Time Waveforms

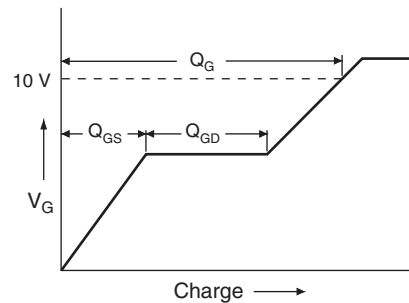


Fig. 17 - Basic Gate Charge Waveform

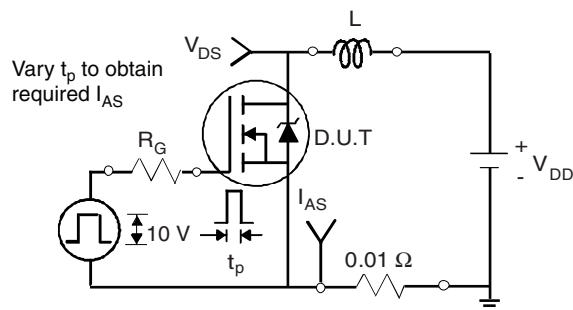


Fig. 15 - Unclamped Inductive Test Circuit

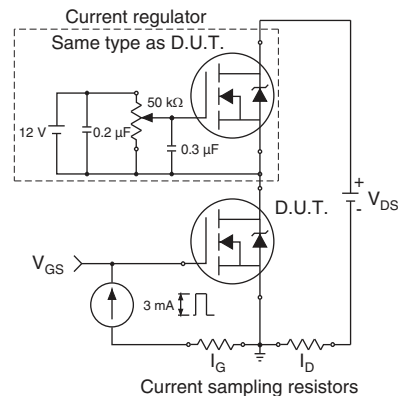


Fig. 18 - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



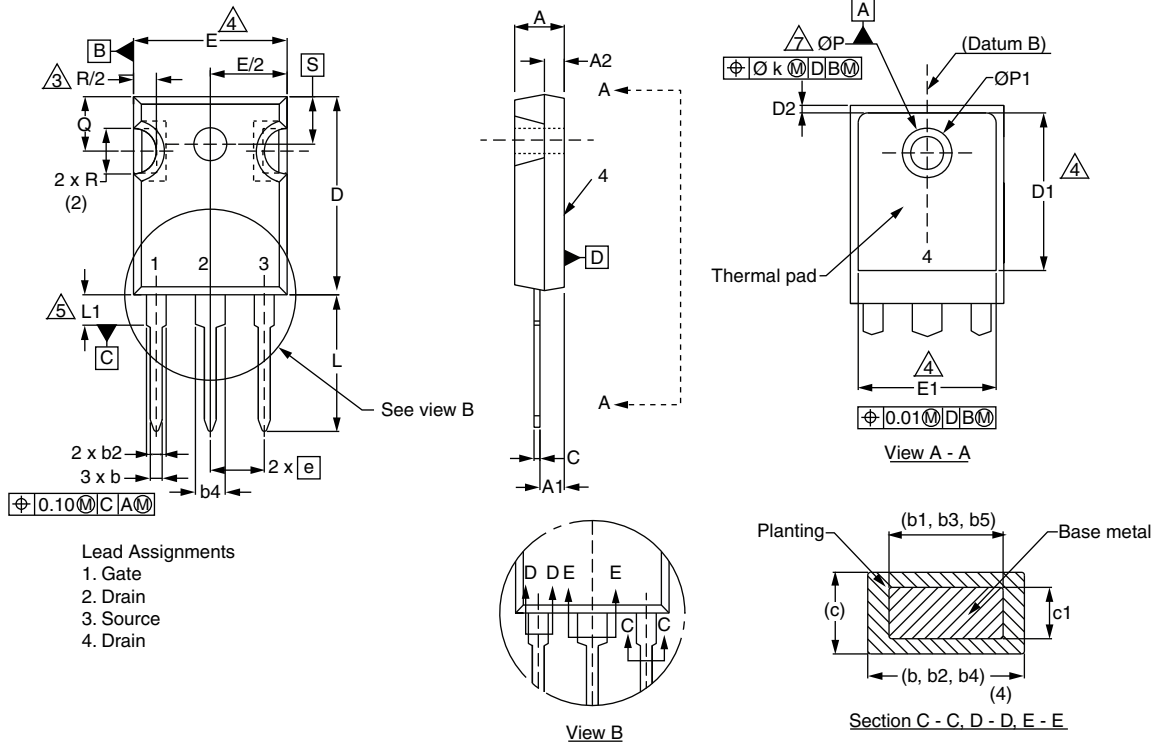
Note

a. $V_{GS} = 5 V$ for logic level devices

Fig. 19 - For N-Channel

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TO-247AC (High Voltage)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.58	5.31	0.180	0.209
A1	2.21	2.59	0.087	0.102
A2	1.17	2.49	0.046	0.098
b	0.99	1.40	0.039	0.055
b1	0.99	1.35	0.039	0.053
b2	1.53	2.39	0.060	0.094
b3	1.65	2.37	0.065	0.093
b4	2.42	3.43	0.095	0.135
b5	2.59	3.38	0.102	0.133
c	0.38	0.86	0.015	0.034
c1	0.38	0.76	0.015	0.030
D	19.71	20.82	0.776	0.820
D1	13.08	-	0.515	-

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D2	0.51	1.30	0.020	0.051
E	15.29	15.87	0.602	0.625
E1	13.72	-	0.540	-
e	5.46 BSC		0.215 BSC	
Ø k	0.254		0.010	
L	14.20	16.25	0.559	0.640
L1	3.71	4.29	0.146	0.169
N	7.62 BSC		0.300 BSC	
Ø P	3.51	3.66	0.138	0.144
Ø P1	-	7.39	-	0.291
Q	5.31	5.69	0.209	0.224
R	4.52	5.49	0.178	0.216
S	5.51 BSC		0.217 BSC	

ECN: X13-0103-Rev. D, 01-Jul-13
DWG: 5971

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Contour of slot optional.
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body.
4. Thermal pad contour optional with dimensions D1 and E1.
5. Lead finish uncontrolled in L1.
6. Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154").
7. Outline conforms to JEDEC outline TO-247 with exception of dimension c.
8. Xian and Mingxin actually photo.





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